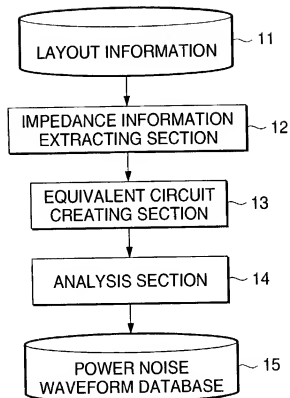


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FIG. 1



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FIG. 2A

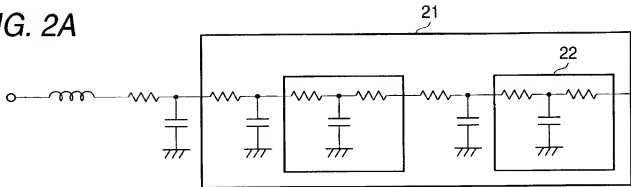


FIG. 2B

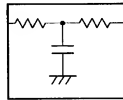


FIG. 2C

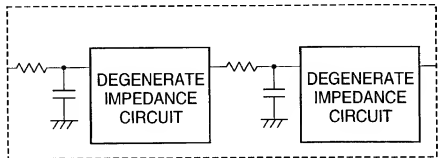
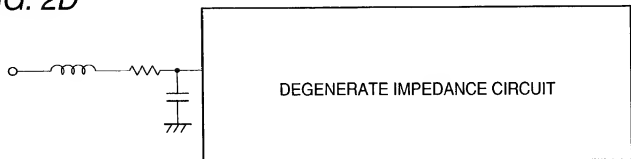
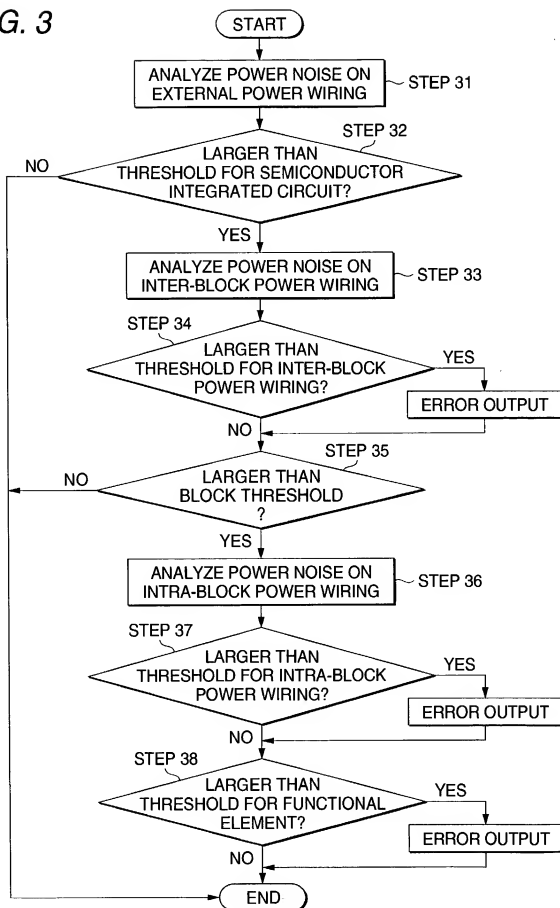


FIG. 2D



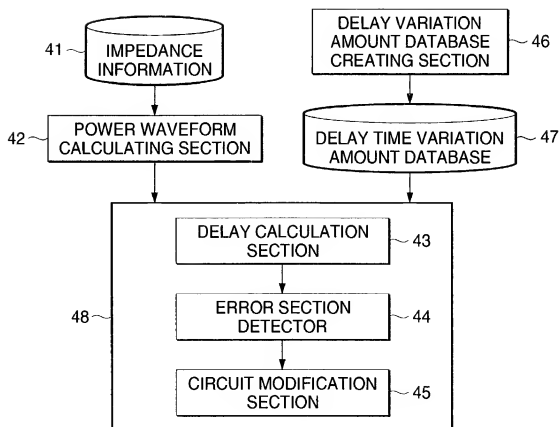
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FIG. 3



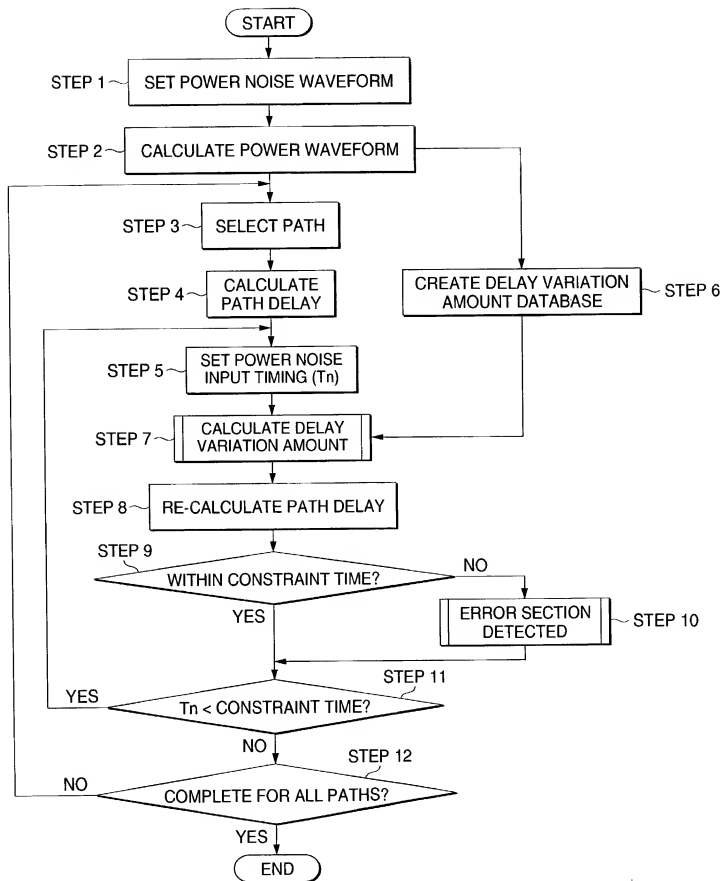
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FIG. 4



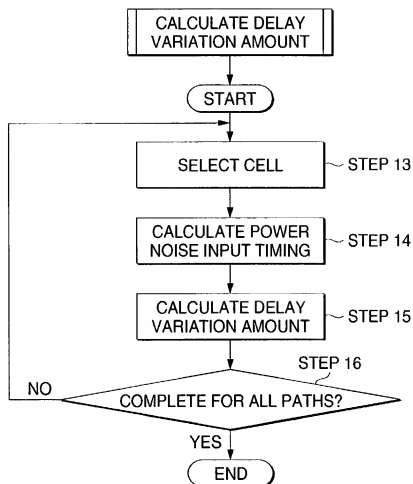
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FIG. 5



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FIG. 6



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FIG. 7

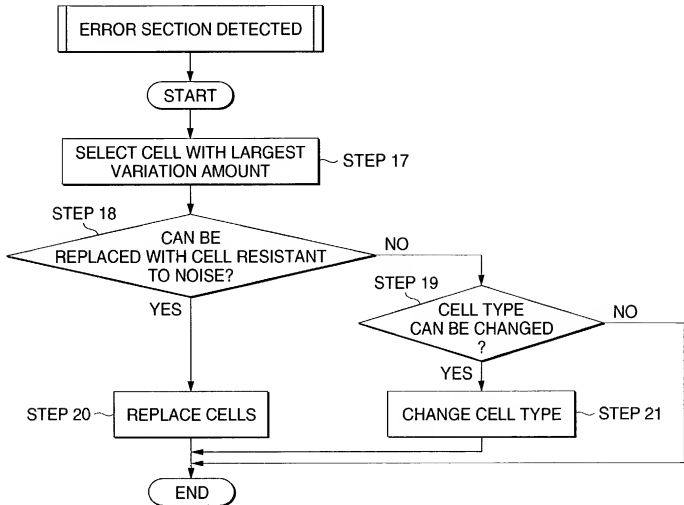


FIG. 8

CELL NAME	PEAK VALUE	DELAY VARIATION AMOUNT PER POWER NOISE INPUT TIMING				
		-20	-10	0	+10	+20
NAND1	10	0	-3	-5	-3	0
NAND1	5	0	-1	-3	-1	0
NAND1	-5	0	+1	+3	+1	0
NAND1	-10	0	+3	+5	+3	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮

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FIG. 9A

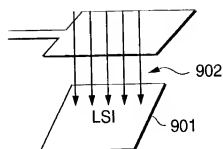


FIG. 9B

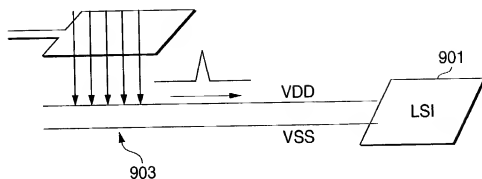
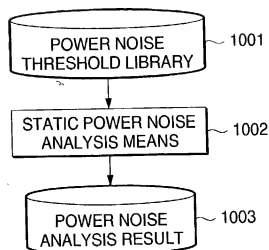


FIG. 10



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FIG. 11A

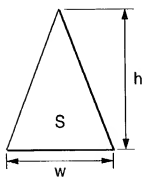


FIG. 11B

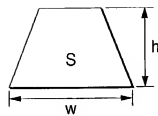
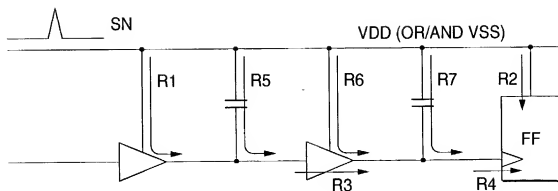
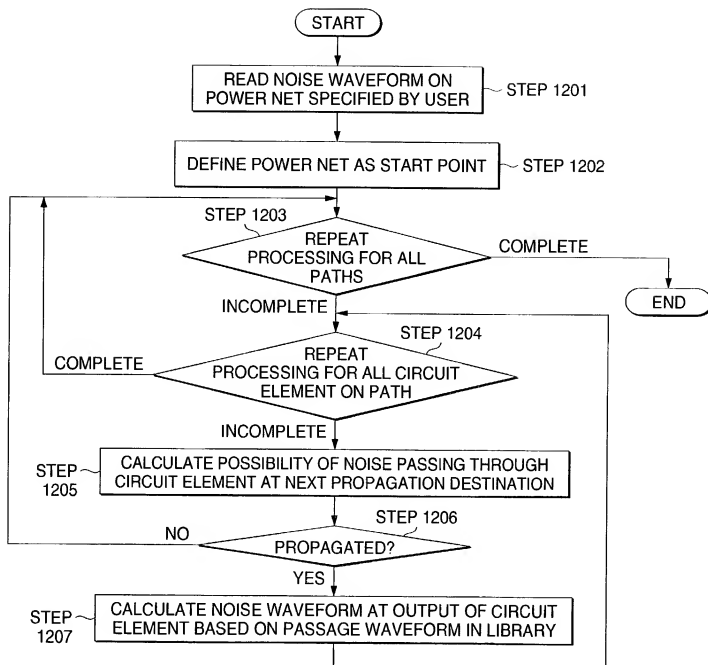


FIG. 11C



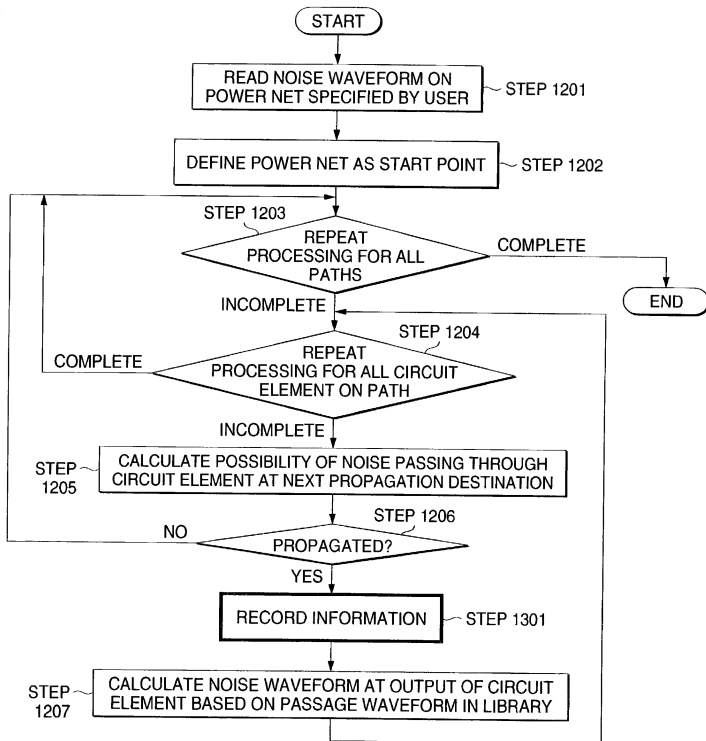
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FIG. 12



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FIG. 13



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FIG. 14

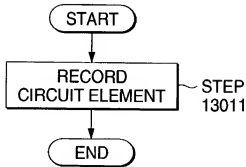


FIG. 15

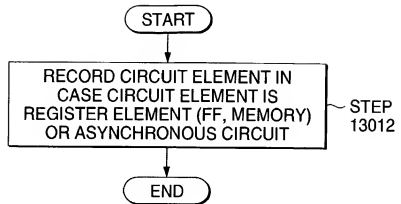
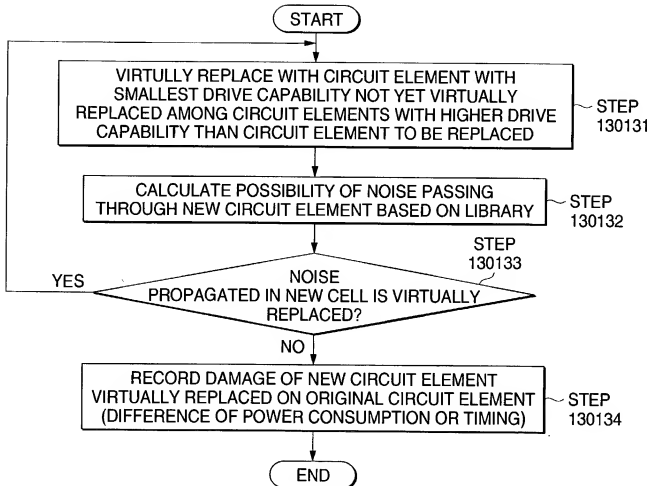
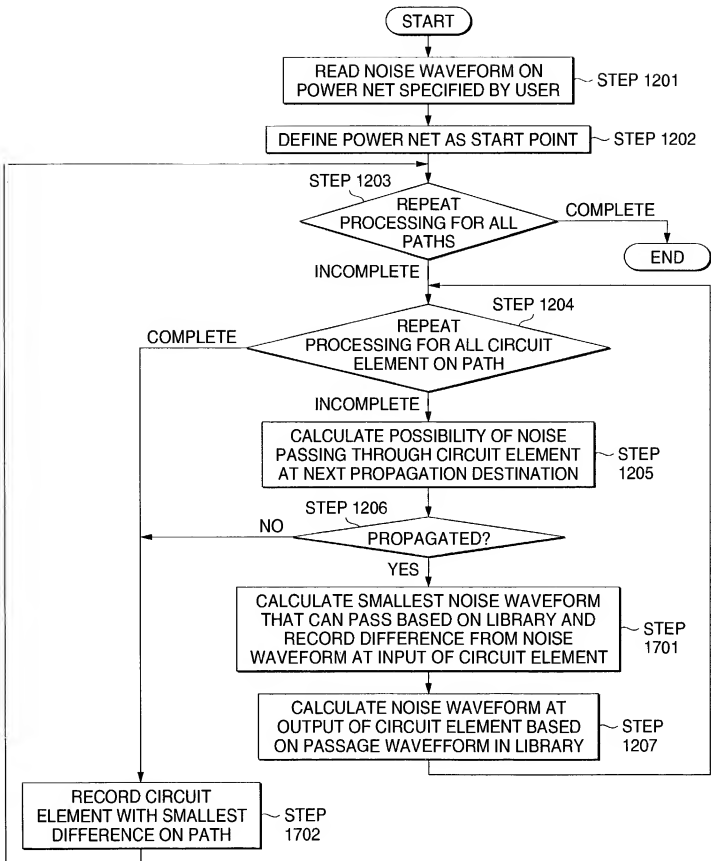


FIG. 16



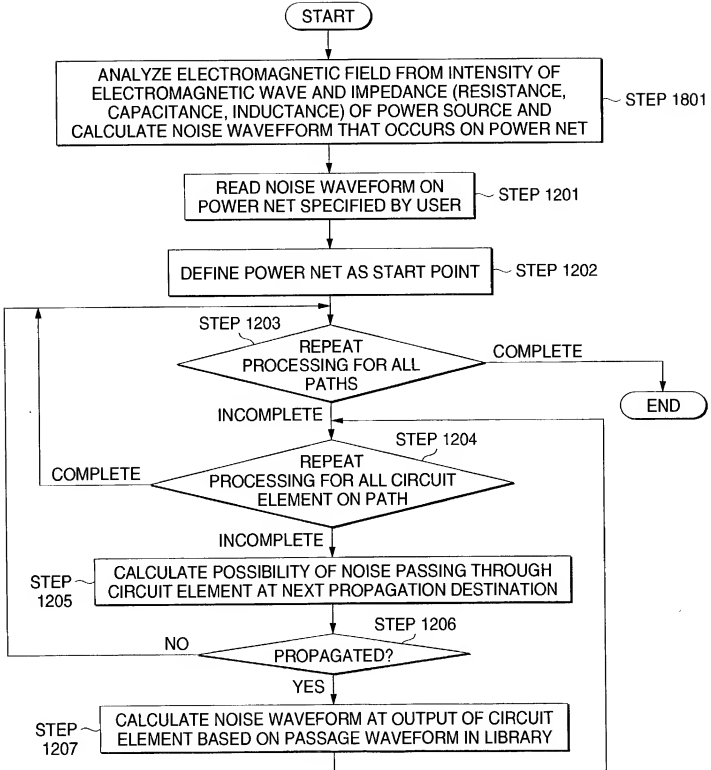
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FIG. 17



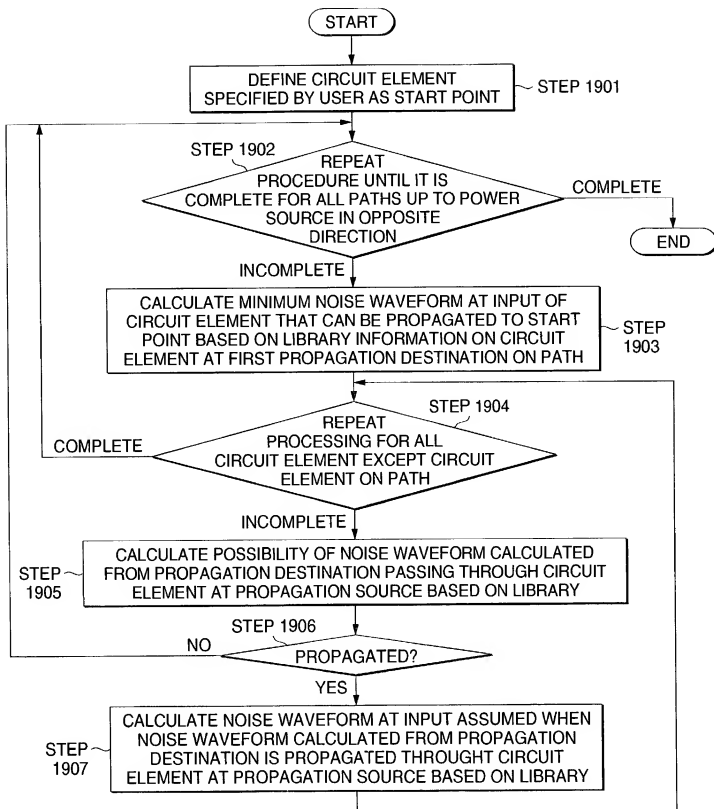
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FIG. 18



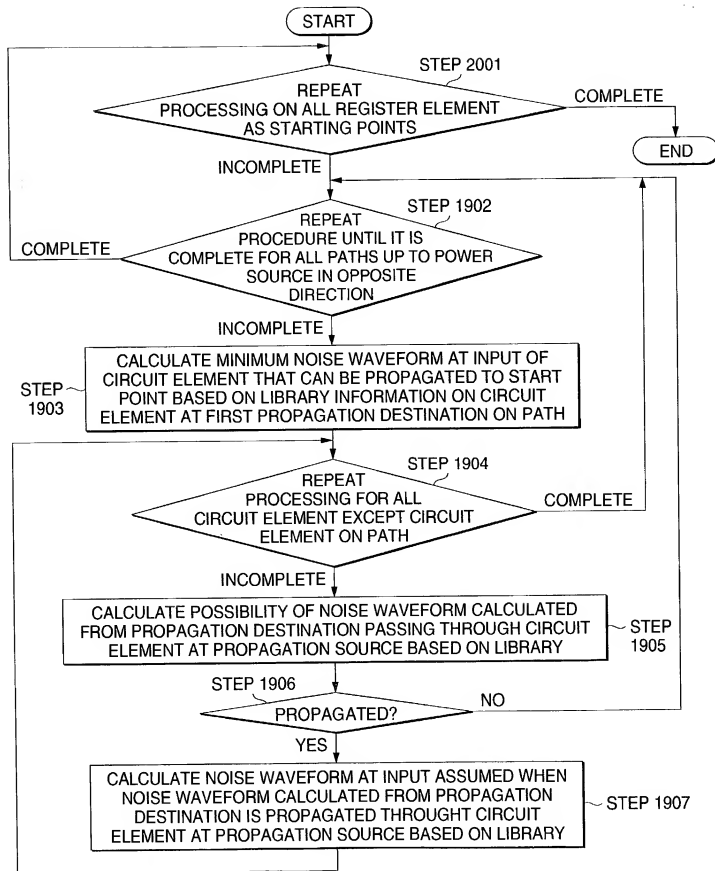
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FIG. 19



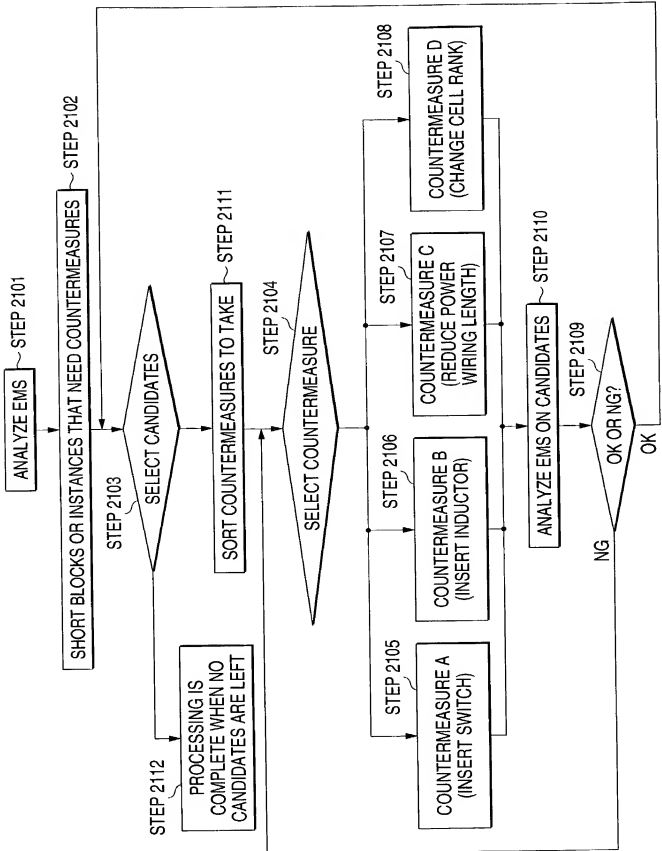
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FIG. 20



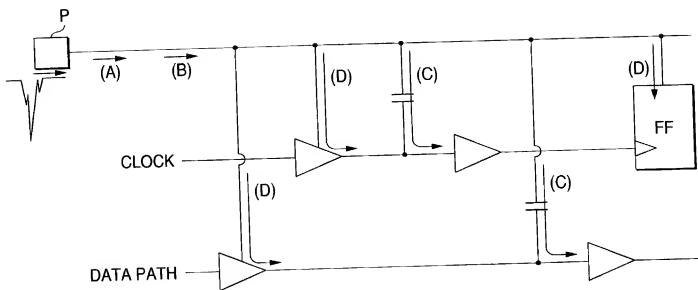
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FIG. 21



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FIG. 22



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FIG. 23

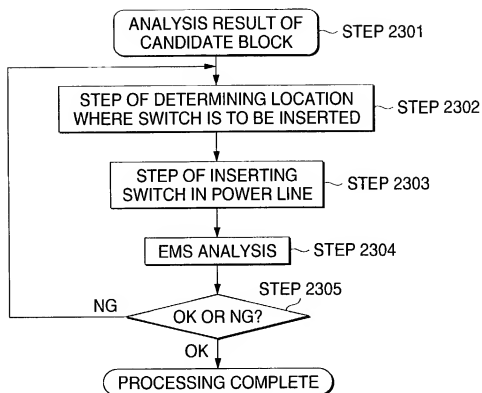


FIG. 24

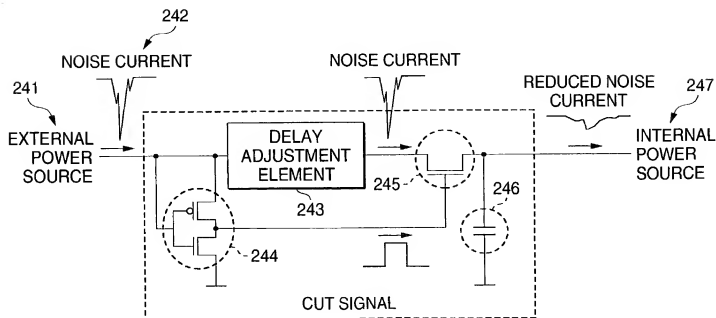


FIG. 25

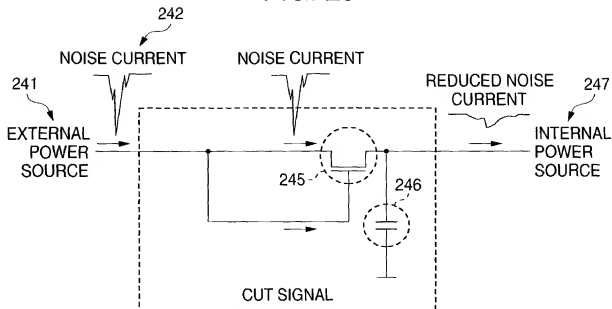


FIG. 26

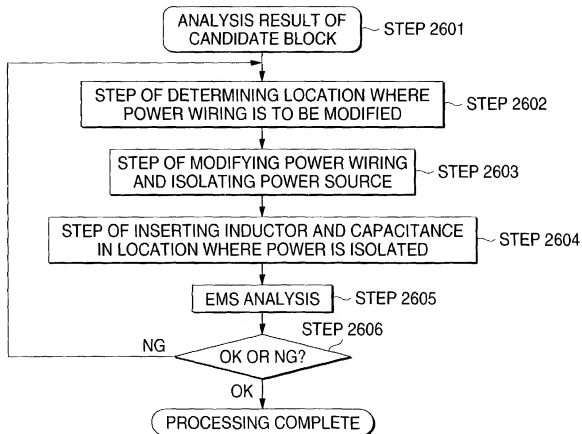


FIG. 27

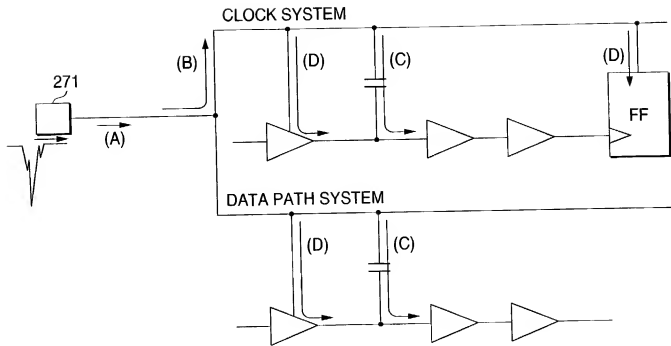


FIG. 28

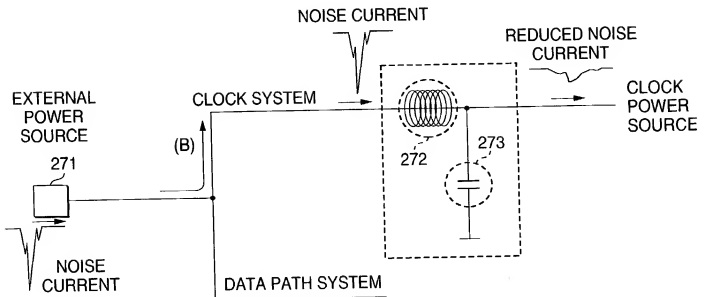


FIG. 29

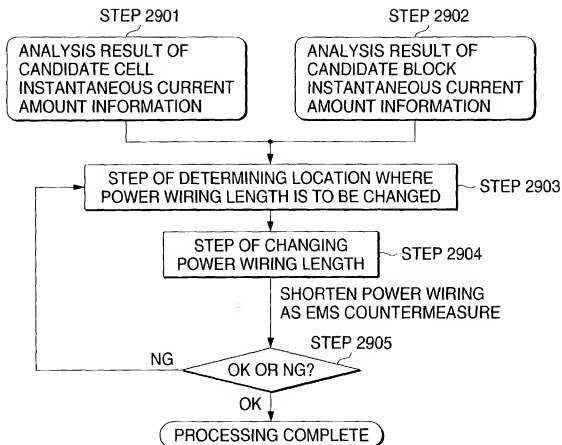
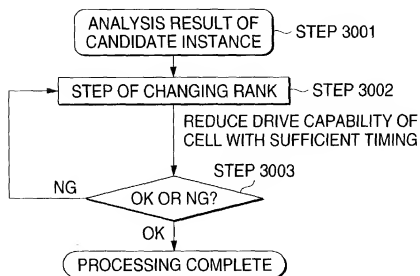


FIG. 30



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FIG. 31

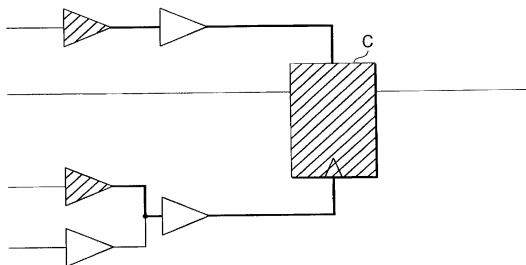
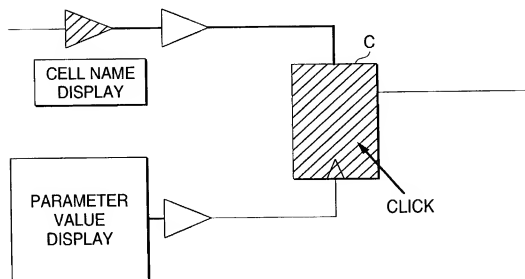


FIG. 32



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FIG. 33

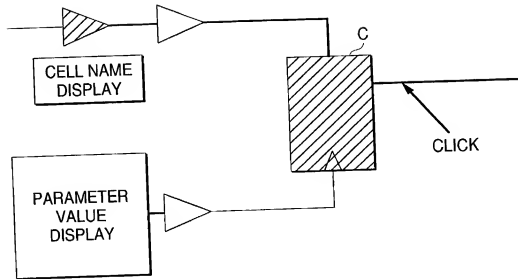
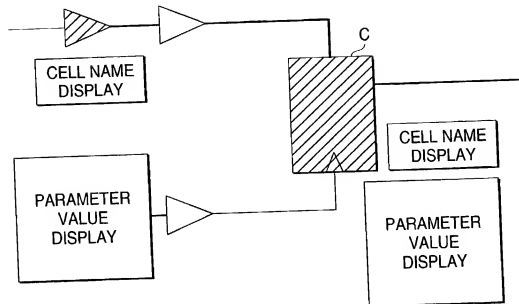
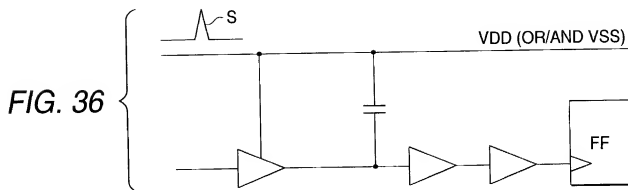
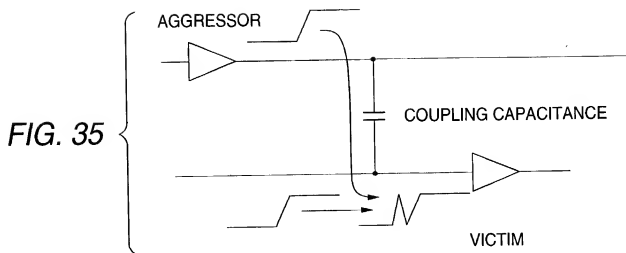


FIG. 34



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**FIG. 37**